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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,081	03/11/2004	Syuji Asano	01-592	4352
23400	7590	12/11/2006	EXAMINER	
POSZ LAW GROUP, PLC 12040 SOUTH LAKES DRIVE SUITE 101 RESTON, VA 20191			LANDAU, MATTHEW C	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

37

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/797,081	ASANO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 15 September 2006.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 7 and 18 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) \_\_\_\_\_ is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, “the areas where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements are identical” (claims 14 and 15) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 9-11, 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 4 and 9, the limitation “a wire interval” renders the claim indefinite. Only one wire has been defined in the claims. Therefore, it is unclear how a “wire interval” can exist.

Regarding claims 14 and 15, the limitation “wherein areas where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements are identical” renders the claim indefinite. It is unclear what is meant by this limitation. What structure is meant to be defined by stating two areas are identical? Identical in what way? What two different areas are being compared? Further, the claims define only one element and/or wire (claim 1 states “at least one of an element and a wire”). The above limitation appears to indicate that Applicant is attempting to claim an element and/or wire below each thin film resistance element.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5, 6, and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiiki et al. (US PGPUB 2002/0020879, hereinafter Shiiki) in view of Nagao.

Regarding claim 1, Figure 1A and 1B of Shiiki disclose a semiconductor device having a plurality of thin film resistance elements 2 through an interlayer insulating film 3 above an area where a wire (4 or 6) is formed on a semiconductor substrate, wherein each of the plurality of thin film resistance elements has a similar shape. As shown in Figure 1B of Shiiki, each resistance element 2 has a rectangular shape. Therefore, it can be considered that each resistance element has a similar shape. Shiiki does not specifically disclose a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate is set to 10 degrees or less. Figure 4 of Nagao discloses a method of forming an interlayer insulating film 403 over wires 401, wherein the upper surface of the insulating film has a small step. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Shiiki by using the method of Nagao for the purpose of obtaining a relatively flat surface (paragraph [0033] of Nagao) without requiring any additional planarization steps, such as CMP. Note that Shiiki discloses using CMP to flatten the interlayer insulating film (see abstract). It is known in the art that CMP has many drawbacks, including high cost. Therefore, eliminating that step would reduce the cost and simplify the production process. A further difference between Shiiki and the claimed invention is the taper angle is less than 10 degrees. However, it would

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have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Shiiki and Nagao by using a taper angle less than 10 degrees, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, Figure 1A of Shiiki discloses the interlayer insulating film 3 is formed so as to cover the overall area below the area where the plurality of thin film resistance elements is formed. It would have been further obvious to use the inorganic SOG film of Nagao (paragraph [0031]), for the purpose of using an insulating material that can function as a good leveling film.

Regarding claim 3, since the step in the insulating film is formed as a result of the underlying wiring 6 and electrodes 4, and that the wiring and electrodes are located under the plurality of resistance elements, it follows that an upper surface of the interlayer insulating film has a higher area adjacent to an area where the plurality of thin film resistance elements is formed than in an area where the plurality of resistance elements is not formed (the area outside of electrodes 1 as shown in Figure 1A). It would have been further obvious to use the inorganic SOG film of Nagao (paragraph [0031]), for the purpose of using an insulating material that can function as a good leveling film.

Regarding claim 5, Figures 1A and 1B of Shiiki discloses the plurality of thin film resistance elements 2 is formed above the area where the wire (4 or 6) is formed, and the thin film resistance elements and the wire are disposed in parallel to each other so that projections thereof are overlapped with each other. Figures 1A and 1B of Shiiki shows layers 2 and 4 (or 6)

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overlap. Whatever portions overlap can be considered the projections. The two layers can be considered parallel since the respective planes in which they reside are parallel to each other.

Regarding claim 6, Figure 1A of Shiiki discloses a plurality of thin film resistance elements 2 located above an interlayer insulating film 3 above an area where a wire 4 is formed, wherein the film is formed to cover the overall area below an area where the thin film resistance element are formed. It would have been obvious to use the inorganic SOG film of Nagao (paragraph [0031]) for the purpose of using an insulating material that can function as a good leveling film.

Regarding claims 9 and 12, the rejection of claims 1 and 3 set forth above similarly applies to these claims. Regarding claim 12, Figure 1A of Shiiki discloses a plurality of wires 4. A further difference between Shiiki and the claimed invention is a wire interval is set to 1.7 microns or more. It would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the invention of Shiiki by using the claimed wire interval range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

*In re Aller*, 105 USPQ 233. It would have been obvious to use a wire interval of 1.7 microns or more to reduce the parasitic capacitance between the wires.

Regarding claims 10 and 11, Shiiki discloses the plurality of thin film resistance elements 2 are formed to have a thickness of 500 angstroms (50nm) (paragraph [0052]), which is within the claimed range of 10-50 nm. Shiiki does not specifically disclose the resistance element has a width between 1 and 10 microns. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the invention of Shiiki by

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using the claimed width range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 13, Figures 1A and 1B of Shiiki disclose the plurality thin film resistance elements 2 further comprises paired thin film resistance elements 2. Note that Figure 1B shows two resistance elements 2 connected by an electrode 1. These resistance elements can be considered “paired”.

Regarding claims 14 and 15, Figures 1A and 1B of Shiiki disclose areas where at least one of the element and the wire is formed below each of the plurality of thin film resistance elements are identical.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiiki in view of Nagao as applied to claims 1 and 6 above, and further in view of Ito et al. (US Pat. 6,770,564, hereinafter Ito).

Regarding claims 16 and 17, Shiiki discloses the plurality of resistance elements comprise CrSiN (paragraph [0051]). Shiiki does not disclose the resistance elements comprise chromium silicon. Figure 4 of Ito discloses a resistance element 3 made of CrSi or CrSiN (col. 3, lines 53-56). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Shiiki by using CrSi as the material for the resistance elements for the purpose of selecting an equivalent material that is known in the art to be used for the same purpose (see MPEP 2144.06).

***Response to Arguments***

Applicant's arguments filed September 15, 2006 have been fully considered but they are not persuasive.

Applicant argues against the drawing objections and 112, 2<sup>nd</sup> paragraph rejections by stating Figures 1 and 2B show the areas below each of the thin film resistance elements are identical. However, Figure 1 shows only one resistance element, so it cannot show the areas below each resistance element. Figure 2B shows more than one resistance element, but does not show the areas below the resistance elements.

Applicant argues that "Shiiki fails to teach or suggest that a plurality of thin film resistance elements are located above the interlayer insulating film, wherein each of the plurality of thin film resistance elements has a similar shape". As stated in the above rejection, Figure 1B of Shiiki does disclose a plurality of resistance elements 2 having a similar shape (rectangular shape).

Applicant argues against the above stated motivation to combine Shiiki and Nagao by stating "Why would one skilled in the art be motivated to use the first and second leveling films 109,110 of Nagao rather than CMP disclosed in Shiiki when Shiiki already appears to achieve a flat surface?". As stated in the above rejection and in previous rejections (such as the Final Rejection mailed on 11/1/2005), the motivation for the combination would be to eliminate additional planarization steps, such as CMP, which is both expensive and complex.

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Applicant further argues that “An electrode 4 and interlayer insulating film 5 are located adjacent to and under the resistance element. So, by the Examiner’s same logic, the adjacent area should not be higher because it follows that an upper surface above the electrode 4 and interlayer insulating film 5 as well should be higher”. The examiner agrees with Applicant that the area above electrode 4 will be higher. In fact, since electrode 4 is the highest point (relative to the other elements below the insulating film 3), the portion of the insulating film 3 above the electrode will also be the highest. Since that area is adjacent to the resistance elements 2, it follows that the insulating film 3 has a higher area (above electrode 4) than the area where the plurality of thin film resistance elements is not formed.

### *Conclusion*

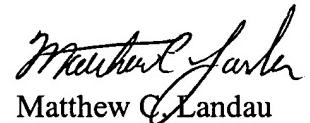
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished

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Matthew C. Landau

December 7, 2006